

ABSTRACT OF THE DISCLOSURE

A memory controller is coupled to a memory device via a memory channel. The memory controller includes a command-per-clock detection unit that compares a portion of a current address with a portion of a previous address. If there is a match, then the memory controller can continue to assert a chip select line coupled to the memory device. The command-per-clock detection unit checks to see whether only certain low-order bits of the address lines are toggling between the current and previous addresses. Additional copies of address lines for particular low-order bits are provided to the memory device to reduce loading on the low order bit address lines, allowing the low order bit address lines to toggle quickly in order to avoid the necessity of inserting a one clock period wait state. If the command-per-clock detection unit does not find a match (meaning that more than the low order address bits are toggling) then the wait state is inserted by deasserting the chip select line for a clock period.